

**IN THE CLAIMS**

1. (previously presented) A semiconductor integrated circuit, comprising:
  - a silicon substrate;
  - a silicon layer that is formed on the surface of said silicon substrate and has a lower resistivity than the resistivity of said silicon substrate;
  - first and second circuit sections formed in said silicon layer; and
  - a device isolation region projecting from said silicon substrate up to a surface of each of said first and second circuit sections between said first and second circuit sections.
2. (currently amended) The semiconductor integrated circuit according to Claim 1, wherein the resistivity of said silicon substrate is between 20 and 100 times ~~or more~~ the resistivity of said silicon layer.
3. (currently amended) The semiconductor integrated circuit according to Claim 2, wherein the resistivity of said silicon substrate is between 50 and 100 times ~~or more~~ the resistivity of said silicon layer.
4. (previously presented) The semiconductor integrated circuit according to Claim 1, wherein said silicon layer is formed of an epitaxial layer.

5. (original) The semiconductor integrated circuit according to Claim 1, wherein a digital circuit is formed on said first circuit section, and an analog circuit is formed on said second circuit section.

6. - 10. (canceled).